

CLAIMS

1. An apparatus comprising:
a substrate having a first elongated edge and a second elongated edge,
wherein the elongated edges are opposite one another;
a plurality of memory devices disposed on the substrate; and
a plurality of channels extending from the first elongated edge to the second
elongated edge, wherein each of the plurality of memory devices is coupled to one
of the plurality of channels.

2. An apparatus as recited in claim 1 wherein the substrate has a first
side and a second side, the plurality of memory devices being disposed on both
sides of the substrate.

3. An apparatus as recited in claim 1 wherein the substrate has a first
side and a second side, the plurality of channels extending across both sides of the
substrate.

4. An apparatus as recited in claim 1 wherein each channel includes a
plurality of conductors, the plurality of conductors following a substantially linear
path across the substrate.

5. An apparatus as recited in claim 1 wherein each channel includes a
plurality of conductors, the plurality of conductors having lengths that are
approximately equal.

1 6. An apparatus as recited in claim 1 wherein the substrate includes a
2 plurality of electrical contacts along the first and second elongated edges.

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4 7. An apparatus comprising:
5 a first substrate having a plurality of memory devices disposed thereon and
6 a first channel portion extending across the first substrate;
7 a second substrate having a plurality of memory devices disposed thereon
8 and a second channel portion extending across the second substrate; and
9 a first connector configured to couple the first channel portion to the second
10 channel portion, wherein the first connector includes a first slot that receives an
11 edge of the first substrate and a second slot that receives an edge of the second
12 substrate.

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14 8. An apparatus as recited in claim 7 wherein the coupling of the first
15 channel portion to the second channel portion through the connector forms a
16 channel.

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18 9. An apparatus as recited in claim 7 wherein the first channel portion
19 extends from a first elongated edge of the first substrate to a second elongated
20 edge of the first substrate.

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22 10. An apparatus as recited in claim 7 wherein the second channel
23 portion extends from a first elongated edge of the second substrate to a second
24 elongated edge of the second substrate.
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1 11. An apparatus as recited in claim 7 wherein the first channel portion
2 includes a plurality of conductors following a substantially linear path across the
3 first substrate.

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5 12. An apparatus as recited in claim 7 wherein the second channel
6 portion includes a plurality of conductors following a substantially linear path
7 across the second substrate.

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9 13. An apparatus as recited in claim 7 wherein the first channel portion
10 includes a plurality of conductors having lengths that are approximately equal.

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12 14. An apparatus as recited in claim 7 wherein the second channel
13 portion includes a plurality of conductors having lengths that are approximately
14 equal.

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16 15. An apparatus as recited in claim 7 further including a third substrate
17 coupled to the first connector.

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19 16. An apparatus as recited in claim 15 wherein the third substrate
20 includes a third channel portion extending across the third substrate.
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1 17. An apparatus as recited in claim 15 wherein the third substrate
2 includes a third channel portion extending across the third substrate, the third
3 channel portion including a plurality of conductors following a substantially linear
path across the third substrate.

6 18. An apparatus as recited in claim 15 wherein the third substrate
7 includes a third channel portion extending across the third substrate, the third
8 channel portion including a plurality of conductors having lengths that are
9 approximately equal.

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11 19. An apparatus as recited in claim 7 further including a second
12 connector having a first slot that receives an edge of the first substrate and a
13 second slot that receives an edge of the second substrate, wherein the edges
14 received by the second connector are on the opposite side of the substrates from
15 the edges received by the first connector.

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17 20. An apparatus as recited in claim 19 wherein the second connector is
18 coupled to a motherboard.

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20 21. An apparatus comprising:
21 a motherboard; and
22 a plurality of pairs of memory modules coupled to the motherboard, each
23 pair of memory modules including:
24 a first memory module having a first channel portion extending
25 across the first memory module;

1 a second memory module having a second channel portion extending
2 across the second memory module; and

3 a first connector coupling the first memory module to the second
4 memory module, wherein the first connector includes a first slot for
5 receiving an edge of the first memory module and a second slot for
6 receiving an edge of the second memory module.

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8 **22.** An apparatus as recited in claim 21 further including a second
9 connector that couples the first memory module to the second memory module.

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11 **23.** An apparatus as recited in claim 21 wherein a channel extends
12 across the first memory module, the second memory module, and the first
13 connector.

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15 **24.** A method comprising:
16 arranging channel portions on a substrate such that the channel portions
17 extend from one edge of the substrate to the opposite edge of the substrate;
18 arranging channel portion conductors such that the length of the channel
19 portion conductors between opposite edges of the substrate is approximately
20 equal; and

21 coupling together a pair of substrates using a connector, a channel
22 extending across the pair of substrates and the connector.

1 25. A method as recited in claim 24 further including propagating
2 signals through the channel.

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4 26. A method as recited in claim 24 further including arranging a
5 plurality of memory devices on the substrate such that each memory device is
6 coupled to a channel portion.

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8 27. A method as recited in claim 26 further including propagating
9 signals through the channel portions to perform memory operations.

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11 28. A method as recited in claim 24 wherein each channel portion
12 includes a plurality of conductors, each of the conductors having approximately
13 equal lengths along the entire length of the channel portion.

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15 29. A method as recited in claim 24 wherein each channel portion
16 includes a plurality of conductors following a substantially linear path across the
17 substrate.

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19 30. A method as recited in claim 24 wherein channel portions are
20 arranged on both sides of the substrate.
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